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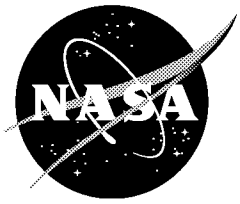

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Study of Conformal Coating on Chip-on-Board Technology for Space Applications

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1.0 Introduction

NASA's New Millennium Program initiatives are aimed at developing miniaturized spacecraft with substantial cost savings. Implementing chip-on-board (COB) technology on Command and Data Handling (C&DH) system can provide a 10:1 weight and volume savings over traditional packaging using hermetically sealed devices on multilayer PC boards. This study evaluated die coating materials that can be used in spaceflight as a die protection against harsh environments. The study evaluated the characteristics of various coating materials and presents the test results of different combinations of the materials under vibration test, temperature cycling test, and temperature humidity bias test.

In COB design, there are three major assembly techniques; namely, chip-and-wire (wire bonding), tape automated bonding (TAB), and flip-chip. Wire bonding technique was chosen in this study, mainly because it is the most widely used technique for electrical interconnection in microelectronic industry; it also supports small volume production, and reworkability. The reliability of wire bonding has been enhanced using gold ball wire bonding and encapsulant. Typically, the wire bonding has an encapsulant over the wires and the die, but this study provided encapsulant protection only on the top surface of the die which permits easier die replacement if required (figure1).

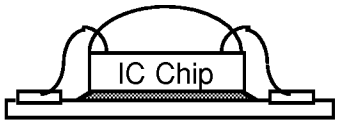

Figure 1. Schematic of wire bonding technique.

Mounting bare die directly on the board requires proper protection to ensure bare die's long-term reliability. A good surface coating material can protect against harsh environments such as moisture, contamination during shipping and handling, mobile ions, and visible and alpha-particle radiation. The conformal coating material requires excellent electrical and mechanical properties for extreme temperature cycling requirements (-55 °C to 125 °C). Evaluating various coating materials benefits COB manufacturers as well as space system designers.

2.0 Known Good Die (KGD)

COB technology can be low cost primarily because of the greater availability and lower cost of known-good-die (KGD). Use of KGD reduces screening and qualification costs and provides high reliability and quality chips. KGD can be purchased from various semiconductor companies, and they generally provide services and tools for testing KGDs, as well as support for the KGD process. There are three main KGD processes: minimal package method, temporary contact method, and soft connection method.

3.0 Die Coating Materials

The preferred choice for coating material should have a high glass transition temperature (Tg ≥ 150 °C) and should have a similar coefficient of thermal expansion (CTE) to that of the bond wire material. The coating material should have excellent adhesion to the die surface to ensure maintenance of the bonding between the assembly and the coating during vibration testing. In addition, since COB technology is often mixed with surface mounted technology (SMT), the material should be compatible with the soldering assembly process.

Ionic contamination can severely damage the COB device and jeopardize its long-term reliability. In the presence of moisture, corrosion from ionic contamination can cause damage to the die interconnect. Selecting a material that has a low ionic contamination content (<20ppm Na^+, K^+, Cl^-) and low moisture permeability is essential.

Commonly used coating materials that are compatible with COB in commercial electronic products are silicone, epoxy, silicon nitride, and parylene. Silicone has low ionic content, low water saturation level, and is thermally stable but has high CTE mismatch, and low glass transition temperature. Epoxy also has low ionic content, high glass transition temperature, high elasticity modulus, comparable CTE match and excellent mechanical protection, but good adhesion characteristics coupled with its high modulus may cause encapsulant cracking. Silicon Nitride has low moisture permeability but a high dielectric constant. Parylene-C is stable chemically and mechanically, is insoluble in all organic solvents and has a uniform coating process, but reworkability is limited.

4.0 Test Vehicles

The memory board and triple track device were used as test vehicles. Test sample dice with or without Silicon Nitride passivation were used in this study. Three different commercially available die encapsulant materials were used for glob-top;

1. Dexter Electronic Hysol FP4402,
2. Dexter Electronic Hysol FP4450, and
3. Dow Corning Silicone Hipec Q1-4939

To support rework, glob-top materials were only applied on the top surface of the die and not the surrounding area. This approach permits replacement of the die without damaging the bond pads on the board. The final conformal coating was applied at the board level with parylene.

4.1 DRAM Board

This memory board depicted in figure 2 is a COB prototype assembly. This assembly consists of four stacked modules forming a 4' by 4' by 2.5" box. Each board uses chip on board and known good die techniques. This unit mirrors the capability of the NEAR and ACE Command and Data Handling boxes. The stacked module design allows incorporation of all spacecraft bus electronics in a single stack with the incorporation of additional modules. This work is being designed and built by Applied Physics Laboratory (APL) in

conjunction with Goddard Space Flight Center (GSFC) and the NASA EEE and Packaging Programs.

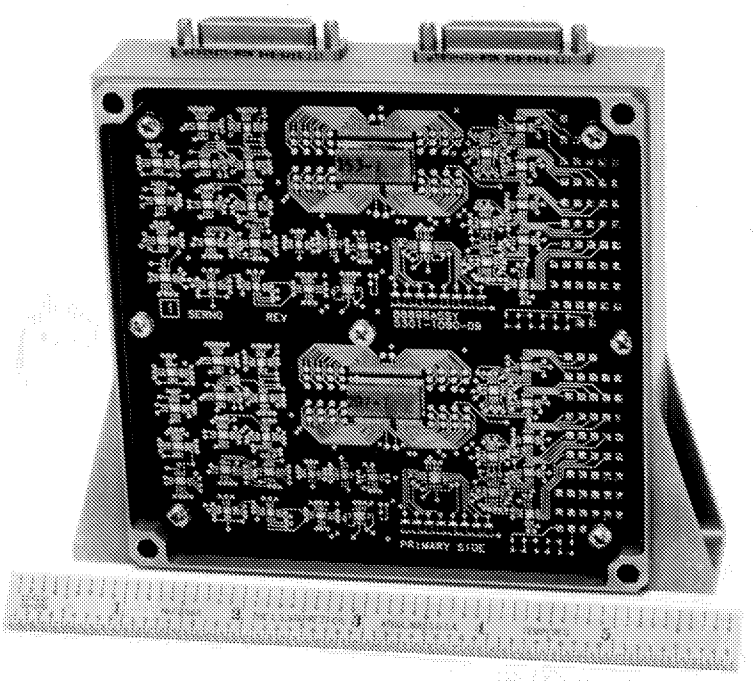

Figure 2. The DRAM board design with 3-D stacked DRAMs for conformal coating evaluation.

A total of eleven DRAM boards were fabricated and covered with a combination of die coating materials with or without a final conformal coating. The combination of the coating materials are listed below (conformal-coating/glob-top/passivation):

1. Parylene/FP4402/-
2. Parylene/FP4450/-
3. Parylene/-/Si_3N_4
4. Parylene/Silicone/ Si_3N_4
5. -/FP4402/ Si_3N_4
6. -/FP4450/ Si_3N_4
7. -/Silicone/ Si_3N_4
8. Parylene/Silicone/-
9. No Coating

Six boards were subjected to dynamic loads test, and a temperature cycling (TC) test. The remaining five boards were exposed to temperature humidity bias (THB) test. The test conditions were as follows:

- Dynamic Load Test: Sine burst test, 50g's @35Hz, 10 cycles, Random vibration test (19.3 G's rms) 20-2000Hz, Shock test (Q=10) 100-10,000Hz
- Temperature Cycling (TC) Test: -55 °C to 125 °C for 1000 cycles
- Temperature Humidity Bias (THB) Test: 85 °C/85 % RH, for 1000 cycles, with bias voltage from -5V to 5V.

4.2 Triple Track Device

The triple track device used in this test is the Assembly Test Chip, version 01 (ATC01) from Sandia National Laboratories. It is designed for use in monitoring integrated circuit damage due to corrosion of aluminum conductors. This test die contains several triple track and ladder test structures. The triple track test structures are very closely spaced parallel aluminum tracks in triplets that run in a serpentine pattern. The resistance of each track can be measured and monitored to detect corrosion. The leakage current between the tracks can also be measured to detect the presence of any conducting path formed by ionic contaminants, dendritic growths or other corrosion agents. Ladder structures are available to characterize corrosion-induced failures quantitatively. A ladder consists of a number of aluminum conductor tracks connected in parallel between two wide metal bus bars. Open paths created due to corrosion effects result in the overall ladder resistance increasing in a stepwise fashion.

Samples used in this test consisted of unpassivated parts as well as parts that have a layer of 7000 Å silicon nitride glassivation. Additional samples without any coating were also included in this test to serve as a baseline for the control samples. Two groups of tests were performed to evaluate the various die-coating materials:

1. A temperature cycling test from -55 °C to +125 °C, and

2. An 85 °C /85% RH temperature humidity biased (THB) test. During the 85°C /85% RH THB test, the triple track structures were biased at 5V from the exterior track to the middle track and at -5V from the interior track to the middle track to accelerate the corrosion process.

A data logger unit was used to record any change in the current passing through the triple track devices. This enabled the detection of any changes in the die behavior. Final electrical performance of the test dice were verified using the Sentry automatic tester at intervals of 100, 250, 500, 750, and 1000 hours of the 85/85 THB test, and at 100, 250, 500, 750 and 1000 cycles of temperature cycling. Table 1 summarizes the coating materials and test matrix.

Table 1 Triple Track Die Coating Test Matrix

Test Sample	First Coating	Second Coating	Test	Note
Un-passivated die	FP4450	None	85^{0}C/85 %RH THB	
Un-passivated die	FP4450	Parylene	85^{0}C/85 %RH THB	
Un-passivated die	FP4402	None	85^{0}C/85 %RH THB	
Un-passivated die	FP4402	Parylene	85^{0}C/85 %RH THB	
Un-passivated die	Hipec Q1-4939	None	85^{0}C/85 %RH THB	Silicone filled
Un-passivated die	Hipec Q1-4939	Parylene	85^{0}C/85 %RH THB	
Un-passivated die	Parylene	None	85^{0}C/85 %RH THB	
Un-passivated die	None	None	85^{0}C/85 %RH THB	Control sample
Die with 7000 Å glassivation	FP4450	Parylene	85^{0}C/85 %RH THB	
Die with 7000 Å glassivation	FP4402	Parylene	85^{0}C/85 %RH THB	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	85^{0}C/85 %RH THB	
Die with 7000 Å glassivation	Parylene	None	85^{0}C/85 %RH THB	
Die with 7000 Å glassivation	None	None	85^{0}C/85 %RH THB	Control sample
Die with 7000 Å glassivation	FP4402	Parylene	-55 ^{0}C to +125 ^{0}C	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	-55 ^{0}C to +125 ^{0}C	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	-55 ^{0}C to +125 ^{0}C	

5.0 Test Result

5.1 DRAM Board Test Result

In the DRAM board test, the test result showed (Table 2) that only one combination, parylene/ Hysol FP4450, passed all environmental tests. Other combination coatings could not complete a full 1000 cycles of THB.

Table 2 Environmental Testing Result of DRAM Boards

	6 boards		5 boards
1st ctg/2nd ctg	**Vibration Test**	**TC Test**	**THB Test**
Parylene/FP4402	Passed	Some Failed	Passed
Parylene/FP4450	Passed	Passed	Passed
Parylene/Si_3N_4	Passed	Passed	Failed
Parylene/Silicone/Si_3N_4	Passed	Failed	N/A
FP4402/ Si_3N_4	N/A	N/A	Passed
FP4450/ Si_3N_4	Passed	Passed	Failed
Silicone/ Si_3N_4	N/A	N/A	Failed
Parylene/Silicone	Passed	Failed	Passed
No Coating	N/A	N/A	Failed

5.2 Triple Track Test Result

Final results from the Triple Track temperature cycling test indicate that all coating combinations with Hysol epoxies successfully passed 1000 cycles. This was not the case for the silicone-coated die, in which high thermal stresses resulting from the CTE mismatch between the encapsulant and the wire bonds caused some wire bond failures. Open circuits started to occur at 250 cycles and the number of wire bonds that failed increased as the test progressed. Table 3 summarizes the test results and figure 3 shows a broken wire bond in the heat affected zone on a silicone coated die.

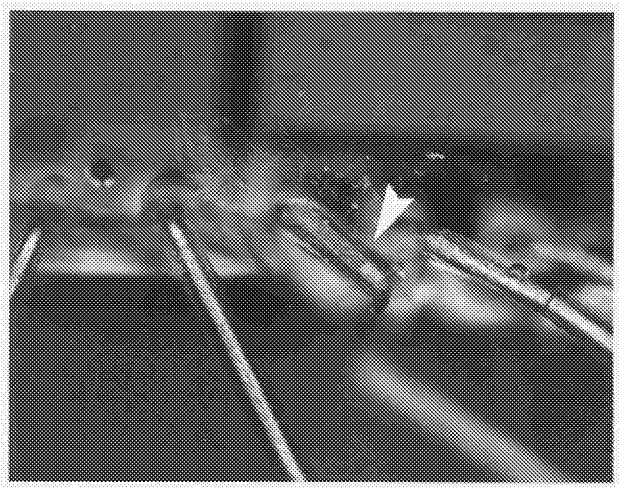

Figure 3. Photograph of a broken wire bond on a silicone coated die.

Table 3. Triple Track Temperature Cycling Test Results

Die Coating	100 Cycles	250 Cycles	500 Cycles	750 Cycles	1000 Cycles
FP4402	Passed	Passed	Passed	Passed	Passed
FP4450	Passed	Passed	Passed	Passed	Passed
Silicone	Passed	17% Failed	57% Failed	81% Failed	86% Failed

In the 85 °C /85% RH THB test, for samples without the manufacturer-deposited passivation, all but one die coating material (FP4402/parylene) exhibited corrosion-related failures. The control samples that did not have any encapsulant protection completely failed shortly after the test started. For dice pre-passivated with silicon nitride at the IC manufacture, all samples coated with Hysol FP4402, FP4450, silicone HIPEC Q14939, or parylene completed the 1000 hour test without any problem. The control samples without encapsulant started to fail at 250 hours. Details of the test results are included in Table 4.

Table 4 The 85 °C/85% RH THB Test Results for Samples with Passivation

Die Coating	250 Hr	500 Hr	750 Hr	1000 Hr
Hysol FP4402/Parylene	Passed	Passed	Passed	Passed
Hysol FP4450/Parylene	Passed	Passed	Passed	Passed
HIPEC Q1-4939/Parylene	Passed	Passed	Passed	Passed
Parylene	Passed	Passed	Passed	Passed
No Coating	44% Failed	44% Failed	46% Failed	75% Failed

6.0 Conclusion

This COB conformal coating study has shown that reliability without hermeticity is achievable using commercially available encapsulant materials. The COB technology has drawn from a multiyear study at JHU/APL in developing viable, economical, and miniaturized electronics. COB technology together with advanced plastic encapsulated micro-electronics provides a viable packaging approach to meet the demand for "better, faster, cheaper" *and now smaller* spaceborne electronics. This research clearly demonstrated that the parylene and epoxy FP4450 combination is the most reliable die coating material of the nine combinations tested. This study has shown that COB technology with appropriate coating has potential for flight qualification.

7.0 Acknowledgment

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13. ABSTRACT *(Maximum 200 words)*

The conformal coating study was initiated by NASA Goddard Space Flight Center as part of collaborative work with The Johns Hopkins University, Applied Physics Laboratory. The objective of this study is to introduce use of Chip-on-Board (COB) technology in spacecraft and propose COB die coating materials for protection against space environment. COB technology was introduced in 1960s and has continued to evolve over the year for consumer electronics market and its popularity has increased in high-reliability applications such as space flight electronics. Since the space technology is continously heading in the direction of increasing functionality, flexibility and density while decreasing weight, volume, and cost, the use of COB technology can accomplish its goal. Its usage in military and aerospace applications will tend to grow once long-term reliability is ascertained. Hence, the extensive conformal coating study was achieved to improve reliability of COB technology.

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